High-Speed Decimal Sub Harmonic Estimation Using a Dual Digital Processor Implementation

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Abstract- With the ever-increased demand for electrical power, use of series compensation scheme is becoming very common in the electrical network. Due to the natural interaction of the series compensation system, occurrence of sub-synchronous resonance (SSR) conditions, sub-synchronous controller interaction/instability (SSCI) conditions and sub-harmonic fero-resonance conditions has become a challenge for the secured operation of the power system. Use of sub-harmonic protection relays is considered as one of the mitigation solutions. High-speed decimal sub-harmonic detection and mitigation is required under certain conditions (such as SSCI) to avoid detrimental consequences of unstably growing sub harmonic. This paper investigates the development of a high-speed sub-harmonic estimation technique using a novel dual processor implementation architecture. The proposed approach involves the use of;

(a) a Field Programmable Gate Array (FPGA), that performs the Recursive Discrete Fourier Transforms (RDFT) at 96 samples/cycle rate (5670 samples/s for the 60 Hz system, 4800 samples/s for the 50 Hz system), and

(b) a Digital Signal Processor (DSP), that performs an adaptive band-pass filtering in the range of 5Hz to 45 Hz, depending on user configurable/selectable sub-harmonics.

Performance of the proposed algorithm has been evaluated using PSCAD & RTDS simulations. Results obtained shows that the proposed method is suitable for fast and accurate detection of sub harmonics resulting from various phenomena.

Keywords: sub-harmonic protection relay, sub-synchronous resonances (SSR), sub-synchronous controller interaction/instability (SSCI), sub-harmonic fero-resonance.

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