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Performance Evaluation of IEC 61850 Process Bus (9-2) Based Distributed Bus Differential Protection Scheme

K. NARENDRA, N. PERERA
ERLPhase Power Technologies, Winnipeg, Manitoba, Canada.

SUMMARY

The paper presents the performance of a novel distributed bus differential protection scheme, which utilizes independent multi-principle advanced protection algorithms, including differential percent slope, delta phase directional comparison, rate of change of differential (ROCOD) currents, delta phase directional comparison on neutral current differential, and a check zone to secure the electrical bus bars up to three zones (two main and one transfer bus).
This bus protection scheme measures currents from conventional CTs, converts them into digital signals and publish them using IEC 61850 process bus based (9-2) sampled values as Merging Unit. It also subscribes the sampled values amongst all the other relay units (within protection scheme) using fiber optic / copper Ethernet communication. High-speed GOOSE messages (IEC 61850, 8-1) is used to monitor the real time Isolator / Circuit Breaker status, enabling dynamic reconfiguration of the CT inputs to different bus protection relay units depending on the load – generation availability. The proposed bus protection scheme does not need any external Ethernet switch for the sampled value (9-2) exchange. Once the sampled values are received by each protection relay unit, they all act as MASTER relays, and all the relays respond (trip/block) simultaneously to the system event. This also adds redundancy into the bus protection scheme.
Rigorous validation and testing has been carried out to validate the performance of the relay scheme using a transmission system simulated in a RTDS (Real Time Digital Simulator). The test cases include switching, loading, inrush currents, and extreme CT saturation conditions for external and internal faults. Many test cases to reflect the practical situation such as high impedance faults, evolving faults, and faults on lightly loaded conditions have also been performed and will be discussed.

KEYWORDS

Bus Differential Protection, sub-cycle, IEC 61850, Sampled Values, Process Bus (9-2), Station Bus (8-1), GOOSE

INTRODUCTION

The Bus Protection forms the vital part of the power system unit protection [1], where the reliability (dependability and security) is paramount as the entire substation power flow will be affected in case of miss operation of the protection scheme. There are many existing bus protection schemes available commercially to protect different bus configurations, but most of these schemes use either the proprietary protocols and/or complicated to understand and implement, and uneconomical. The purpose of this paper is to present a multi-principle microprocessor based advanced bus protection scheme, which utilizes the international standard protocol (IEC 61850) for the exchange of sampled values (9-2) and the high speed GOOSE messages (8-1) to reflect the dynamic replica of the Isolator and Breaker status for monitoring different zones of bus protection. The proposed advanced microprocessor based bus protection scheme does not require current inputs from Merging Units; instead, it has the ability to measure the conventional CT currents within the protection unit, and will share / distribute the sampled values using IEC 61850, 9-2 protocol, as a Merging Unit with other protection units to perform the overall differential protection. Each protection unit therefore acts as a processing (subscribing sampled values) and as well as a Merging Unit (publishing sampled values). The scheme can be scaled to support up to 24 bays (24 sets of three phase CT current inputs) and a three phase PT voltage input with 4 individual relay protection unit (6 sets of three phase CT current Inputs) functions together as one protection scheme, in a very compact electrical panel (4 x 3U rack units). For time synchronization, additional inputs, and outputs, an I/O unit is used to accommodate the breaker status, isolator status, and any other inputs into the bus protection scheme.

This advanced bus protection system measures currents from the conventional CTs and also publishes the IEC 61850 process bus based (9-2) protocol to exchange the sampled values amongst all the units using fiber optic / copper Ethernet communication. The IEC 61850 station bus (8-1) with high-speed GOOSE messages are also used to monitor the real time Isolator / Circuit Breaker status which allows for the dynamic reconfiguration of the CT inputs to different bus protection relay unit depending on the load – generation availability. The proposed bus protection scheme does not need any external Ethernet switch for the sampled value (9-2) exchange.

Easy to use User Interface Windows software is used to set the Relay settings and for viewing Events, Fault logs, real time metering, and recording from any Relay unit. One logical recording will display all the channels (upto 24 bays), phase segregated differential protection quantities (operating and restraining) for further analysis. User definable logics further enhance customization capability with the available internal protection Relay logics. Rigorous validation and testing has been performed using advanced RTDS (Real Time Digital System) and field captured COMTRADE file playback for switching, loading, inrush currents, extreme CT saturation conditions for external and internal faults. Many test cases for high impedance faults and faults on lightly loaded conditions have also been verified and will be discussed.

IEC 61850 ARCHITECTURE

The IED (Intelligent electronic device) is refereed below as bus protection relay unit, which can take upto 6 sets of three phase input currents as shown in Figure 1. The proposed bus protection scheme can be scaled to support upto 4 individual IEDs to protect upto 24 bays, with three independent zones. The following Figure 1 uses only two IEDs for illustrative purpose.

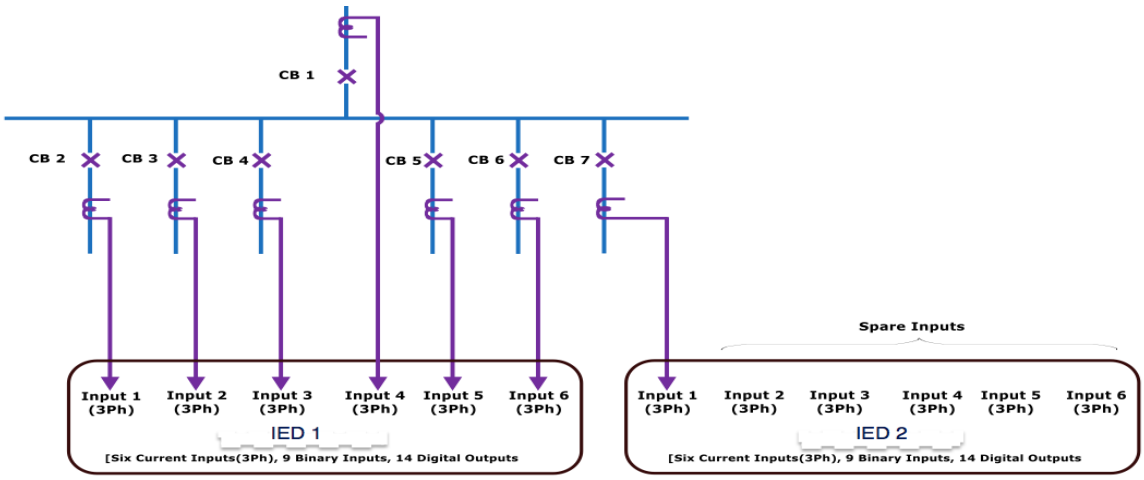

Figure 1: Illustrative 7 bays system with two IEDs for bus protection.

As mentioned in the previous sections, an additional I/O unit (Input / Output unit), which is also an advanced microprocessor device, is used which has dual role to play. The important function of this I/O unit is to provide a common time reference signal to all the bus protection IEDs in the form of 1PPS (pulse per second) to do synchronized sampling. The other important function of this I/O unit is to provide Isolator/Circuit Breaker status with a capability upto 128 additional digital inputs and 16 output contacts. The time synchronization function will be explained in the later section in detail.

NETWORK ARCHITECTURE FOR SAMPLED VALUE (9-2) AND GOOSE (8-1) EXCHANGE

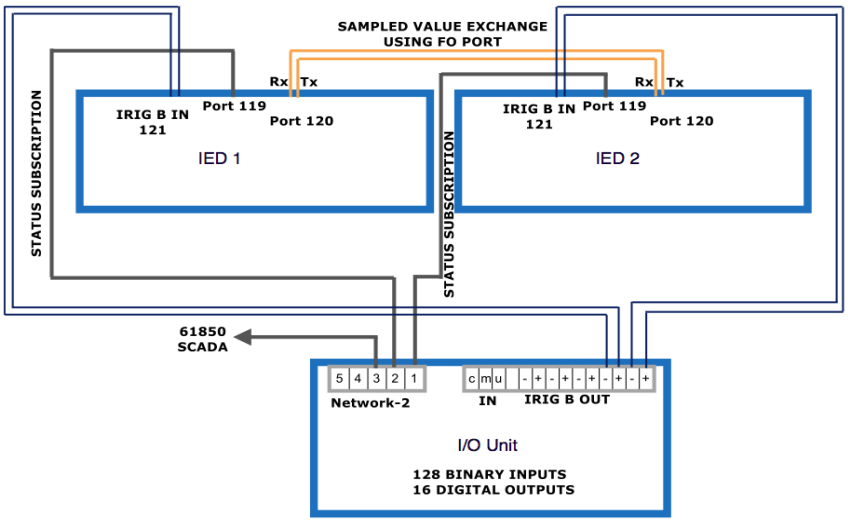

Figure 2: The network architecture for sampled value (9-2) and GOOSE (8-1) data exchange.

In the above Figure 2, an illustrative two IED system with an I/O unit and its network connectivity is depicted. The Sampled Value exchange as per IEC 61850 (9-2) protocol can be accomplished using either fiber or copper Ethernet port, and additional external Ethernet switch is not essential. Similarly, the Isolator /Circuit Breaker status can be exchanged using high speed GOOSE messages as per IEC 61850, 8-1over other Ethernet (fiber or copper) port available on the IEDs and the I/O unit. External Ethernet switch can also be used to accomplish the sampled value and GOOSE exchange. The RMXU standard logical node as defined in IEC 61850, 7-4 ed 2 has been used for the sampled value exchange between different IEDs. In the proposed implementation, the sample rate used is 8 samples / cycle of the system

frequency (50 or 60 Hz). The CT inputs are sampled at much higher rate (96 samples /cycle), but for the differential protection, it is sufficient to have 8 samples / cycle. Therefore, there will be a down sampling done from 96 samples / cycle to 8 samples / cycle before the samples values are exchanged using the above logical node.

THE PUBLISHER AND THE SUBSCRIBER ARCHITECTURE

Each IED has two services for the sampled value exchange. The SAV publisher will publish a MSVCB with 6 RMXU logical node information along with additional digital word in the data set. Totally, there will be 19 words of data that will be published using SAV publisher service from each IED. On the subscriber service, the SAV Subscriber will receive up to 57 words of data (essentially from three IEDs each publishing 19 words). The sampled values are checked for the data integrity and the time alignment before it is passed onto the protection algorithm, which is executed 8 times in one cycle of system frequency (50 or 60 Hz). In the event of late arrival of the sampled value packets (or missing data), bad data, miss alignment due to time synchronization, the protection algorithm will block the Relay operation and provide alarms for the appropriate events.

Once each IED (protection relay unit) receives the sampled values measured by rest of the other units, they all act as MASTER-MASTER relays, and all the relays respond (trip/block) simultaneously to the system event. This also adds redundancy into the bus protection scheme, and user can further enhance the logic by implementing the VOTING scheme or any other logics using enhanced user definable easy-to-use "PROLogics". The tripping time for 5 times the nominal value magnitude of the fault current for 24 bays is less than 9 milliseconds, which assures the sub-cycle operations for 50 or 60 Hz system.

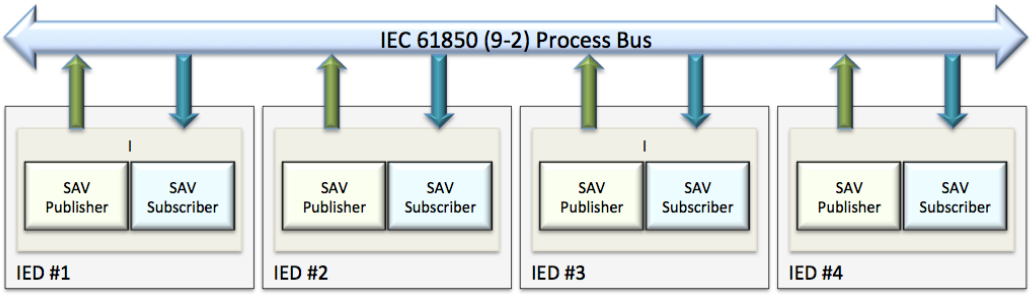

Figure 3: The sampled value (SAV) subscriber and publisher architecture used in each bus protection IED.

TIME SYNCHRONIZATION

A reliable time reference signal (which does not depend on the external time sources – such as GPS signal) is generated with an I/O unit to ensure the sampling synchronization and data alignment. External time sources such as IRIG-B, SNTP are also supported, if available, but are not essential for the differential protection. The simultaneous sampling time accuracy is +/- 5 micro seconds (around 0.1 degree). Various alarms will be generated for the unit synchronization / communication issues and appropriate blocking action will be performed instantaneously to secure the bus.
As shown in the Figure 4, the time synchronization starts with the I/O unit generating 1 PPS within the unit with reference to the free running real time clock (RTC). Later, this time is distributed to all the IEDs (protection units) to have common time reference using IRIG-B output from the I/O unit, which will be received by all the IEDs using their IRIG-B input. If the I/O unit receives any IRIG-B input from the external GPS clock or other resources such as SNTP, the same will be utilized to generate the IRIG-B output and will be distributed to the IEDs. The time distribution will happen seamlessly whether external

GPS clock is available or not and hence the protection system does not depend on any external GPS clock signal or time reference. This is important for the reliability of the protection.

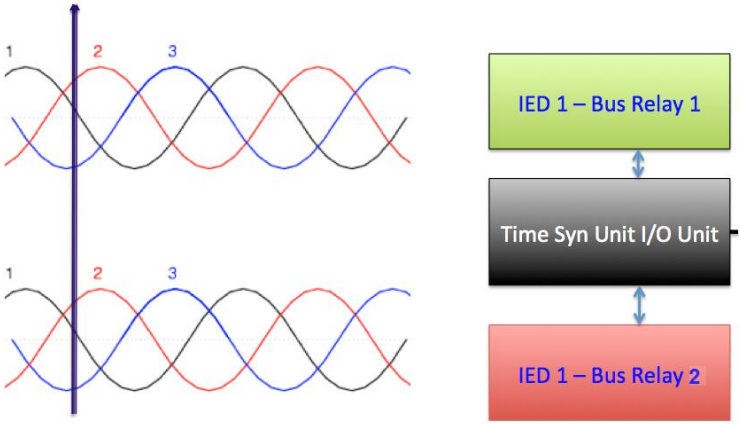

Figure 4: The time synchronization concept with two IEDs and an I/O unit

SIMULATIONS AND RESULTS

In order to evaluate the performance of the proposed implementation, several test cases have been simulated using the RTDS and results are summerized below.

Case-1 : 24 bays performance for 5 times the nominal pickup – Internal Fault.

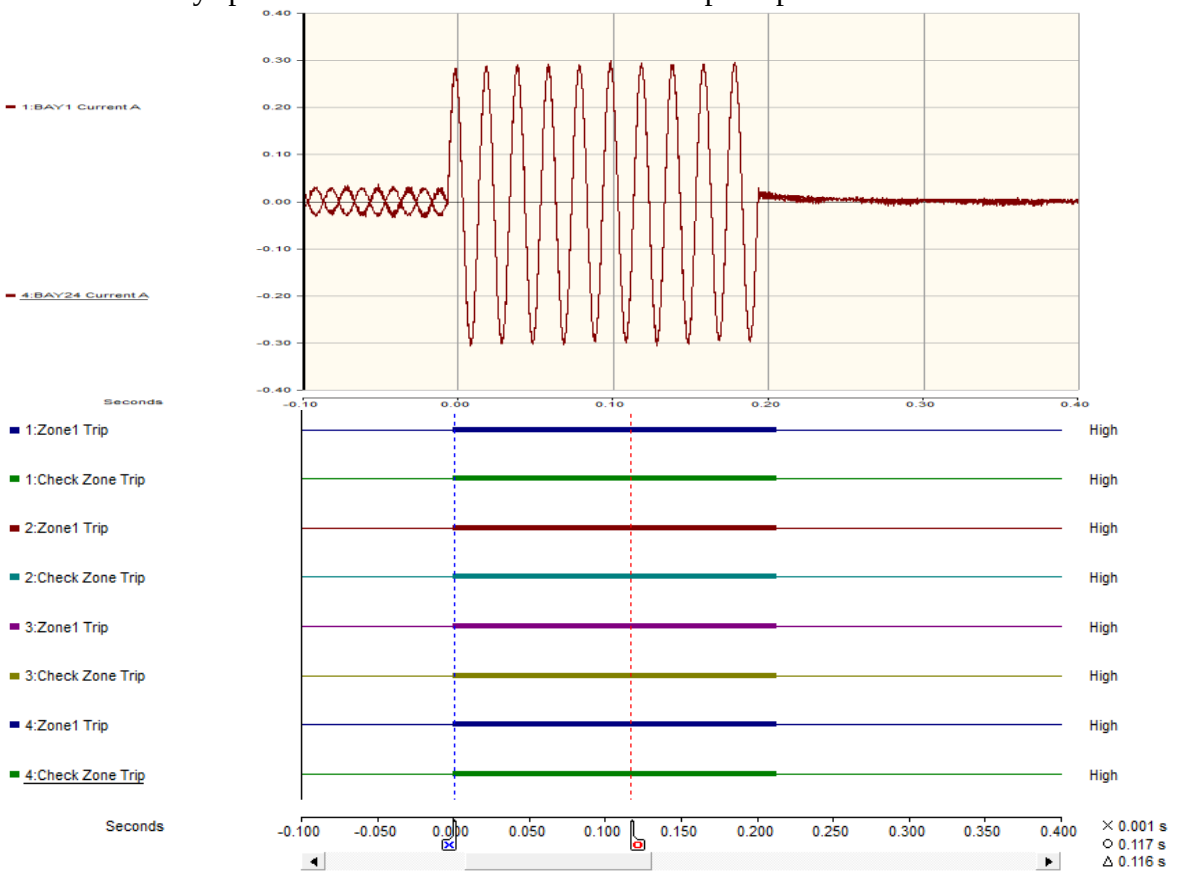

Figure 5: The 24 Bay differential protection operation within 9 mili-seconds after the fault inception.

Figure 5 shows the operation of differential protection of Zone-1 for an internal fault simulated on a 24 bay system with a fault current of 5 times the nominal pickup. All the IEDs have operated as desired within 9 milli second after the fault inception. This clearly shows the response capability of the proposed bus scheme in terms of the sub-cycle operation even with fault current levels of only 5 times the nominal.

Case-2 : Evolving external fault into internal bus fault.

Figure 6 shows the operation of the relay for an evolving fault. As can be observed, the high miss match principle it self is not sufficient to secure the bus as the miss match (traditional percentage slope) has happened much earlier and would have miss operated the relay. As the proposed relay uses multi-principles to secure the bus and as desired the relay has operated correctly when the fault has evolved as an internal fault in the bus zone.

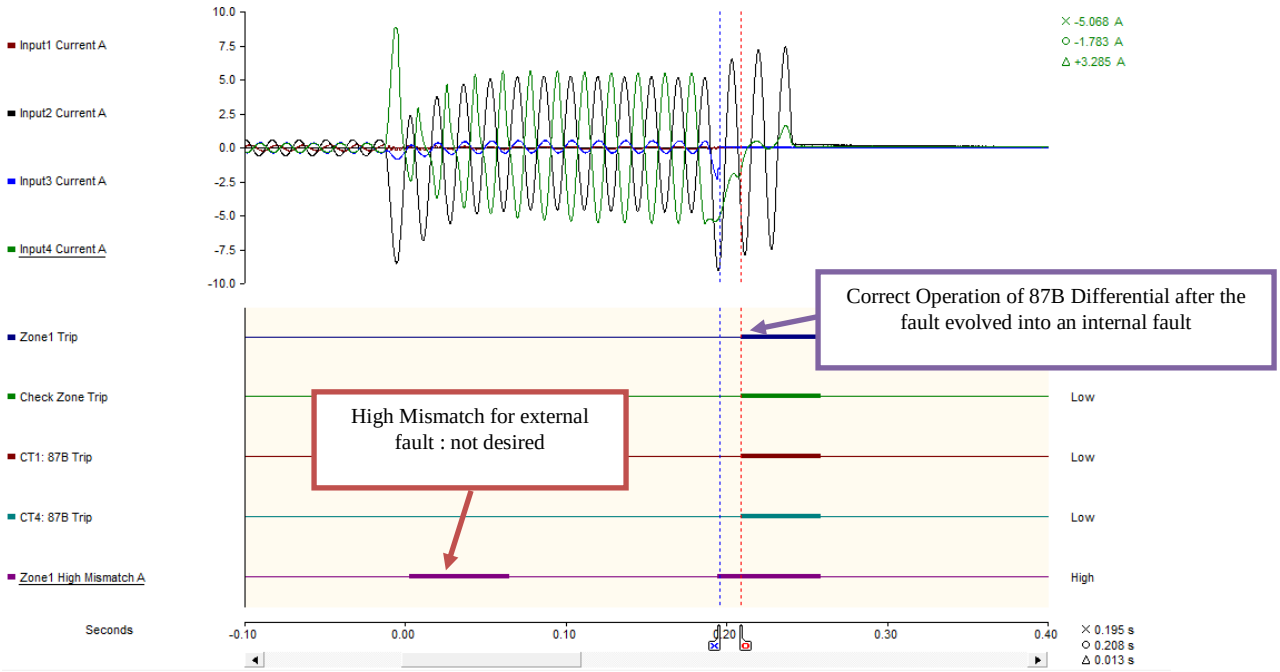

Figure 6: Evolving fault from external to internal bus zone.

Case-3 : Extreme CT saturation during external fault.

Figure 7 shows the bay 1 and bay 2 currents with extreme CT saturation. Due to the phase angle comparaison principle used (delta-phase), it can be seen that the bus protection scheme is very secured against the CT issues, and hence the protection scheme is in sensitive to the errors in the CTs and hence has low dependency on the accuracy of the CTs. Hence the relay secures the bus during external fault even with extremely distorted currents since it uses multi-principles, which are independent of each other.

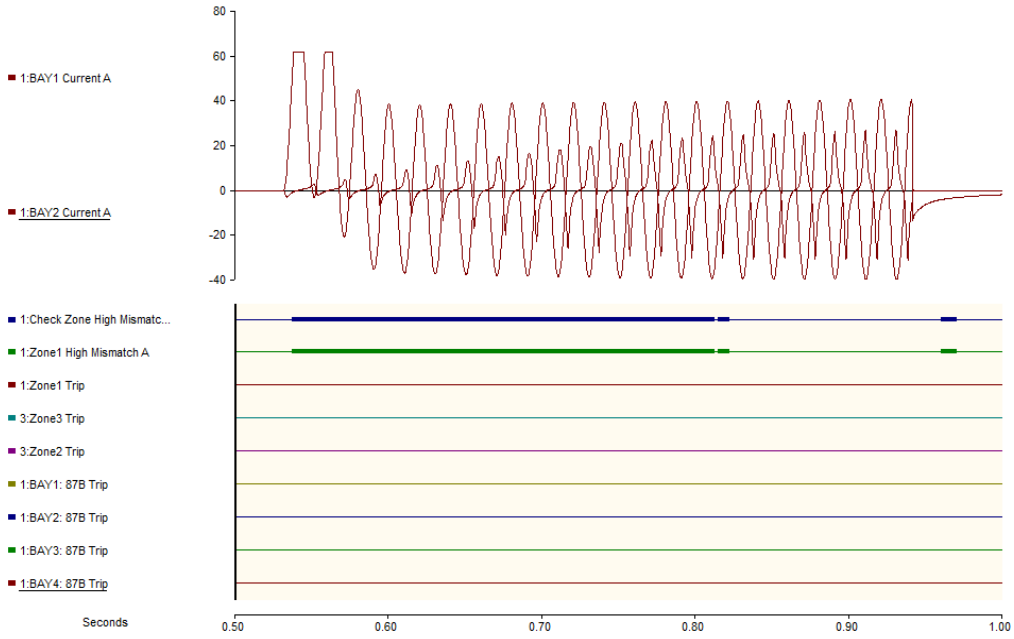

Figure 7: Extreme CT saturation with external fault.

Case-4 : Energization of transformer during internal fault.

The following case shows the performance of the proposed relay during the energization of the transformer connected to the bus and during that time an internal fault occurs. Here again, the relay is very selective and tripped the bus due to the internal fault within 7 milli-seconds. Figure 8 shows the zone 1 trip, check zone trip along with the high miss match current.

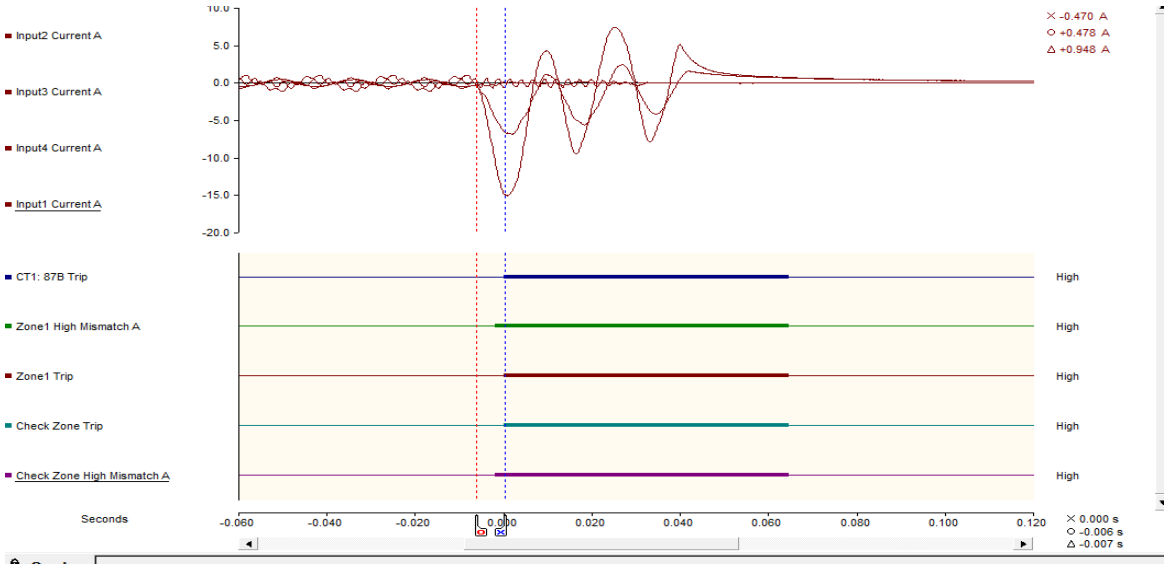

Figure 8: Transformer energization during an internal fault

CONCLUSTIONS

A microprocessor based bus protection scheme, which utilizes the international industry standard IEC 61850 protocol for the sampled value (9-2) and high speed GOOSE (8-1) has been presented. The relay uses multi-principles to secure the bus against CT saturation, inrush currents, transformer energization, and other anomalies. Performance of the proposed relay was evaluated using various test scenarios simulated using RTDS. Result obtained showed that the proposed scheme reliably operates with security and dependability on the internal fault with extremely distorted currents from the CTs. The proposed scheme is scalable, flexible and very easy to use.

BIBLIOGRAPHY

[1] "Electrical Bus Protection Method and Apparatus", Dave FedirChuk et. al, US Patent - 7,199,991 B2, Issued April 2007.
[2] Krish Narendra, Dave Fedirchuk, "Secured Busbar Differential Protection Using A Computationally Efficient Dot Product Technique", Conference on Power System Protection and Automation, New Delhi, India, 2010.
[3] Narendra, Krishnaswamy Gururaj; Swift, Glenn William; Fedirchuk, David James; Neufeld, Arthur, "An efficient method for calculating the dot product in fault detection algorithms", US Patent application 12/753,020, pending.
[4] Bogdan Kaztenny, Gustavo Brunello, Lubomir Sevov, "Digital low impedance bus differential protection with reduced requirements for CTs", IEEE Transaction, 2001, pp 703-708.
[5] Narendra, Krishnaswamy, Gururaj; Fedirchuk, David James; Zhang, Nan, "Rate of change differential protection", US Patent Application, 13/350,070, pending.
[6] Zhying Zhang, Krish Narendra, Dave Fedirchuk, G. Punnose, Premnath, "A novel CT saturation detection algorithm for bus differential protection", CIGRE, November, 2008.
[7] Yong-Cheol Kang, Seung-HunOk, Sang-Hee Kang, "A CT saturation detection algorithm", IEEE Transaction on Power Delivery, Vol 19, Jan 2004, pp 78-85.
[8] Lubomir Sevov, Bogdan Kaztenny, Ed Taylor, "Commissioning and testing complex busbar protection schemes – experience at pacific Gas & Electric", 60th Annual Georgia Tech Protective Relaying Conference, Atlanta, Georgia, May 3-5, 2006, pp 1-16.