A NOVEL CT SATURATION DETECTION ALGORITHM FOR BUS DIFFERENTIAL PROTECTION

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***Abstract* - This paper presents a novel algorithm (patented) for detecting the early CT saturation in bus differential protection, which, combing with the late CT saturation block zone and other security enhancement features provides great securities to the bus differential relay on external faults, and also maintains the relay with high sensitivity and fast operation for internal faults.**

Index Terms – CT saturation, Bus protection, 87B Differential Protection

1.0 INTRODUCTION

CT saturation is not uncommon in bus differential protection. Many literatures are available [1],[2],[3],[4], which describes this phenomenon, especially during external fault conditions. Microprocessor relays are generally considered as low impedance relays. The analog inputs (primary current) to these relays are from the station CTs and to match the required voltage to the microprocessor level, the currents are further stepped down on the relay using smaller CTs. Bus protection involves various configurations of the terminal devices which typically include feeders, transformers, generators, and the combinations of various devices. There are different protection methods or philosophies available to protect a bus – bar element in power system. The most commonly used method in micro processor relays is based on the percentage differential scheme. In this paper, a novel CT saturation algorithm [5] (patented) will be described which is realized by evaluating the phase relationship of the first derivative (i.e. dIO/dt and dIR/dt) of the readily available operating current (IO) and the restraint current (IR) in bus differential protection. For an internal fault, both IO and IR start to increase simultaneously and the phase angle between dIO/dt and dIR/dt is very small and can be considered to be in phase. For an external fault with CT saturation, no matter how severe and how soon the CT starts to saturate, the phase angle of dIO/dt is always lagging with respect to dIR/dt. The use of the derivative calculations (dIO/dt, dIR/dt) is to capture the IO, IR trajectory movement sensitively, quickly and accurately. This algorithm has been tested thoroughly by using the real time digital simulator (RTDS). The test results have showed that this algorithm works correctly and reliably for all the test cases (internal/external, with/without CT saturation, early CT saturation or late CT saturation, etc.). The test results also showed that this algorithm is immune to harmonics, DC offset, line angle, fault types and fault arcing resistance. This paper will present some of these test results.

2.0 MOTIVATION TO THE NEW ALGORITHM

With the availability of faster digital signal processors at lower cost, it is not difficult to implement various schemes to encounter the challenges posed by the legacy measuring systems. The station CTs are generally designed to meet all possible fault conditions. Many off-line studies are conducted prior to the implementation of the protection scheme. However, there are circumstances, which are beyond control, which can pose challenges to advanced microprocessor technology. It is not uncommon that the electrical bus protection relays are subject to severe saturation due to external fault currents. The motivation to this algorithm is the CT saturation caused during external fault, which is described below.

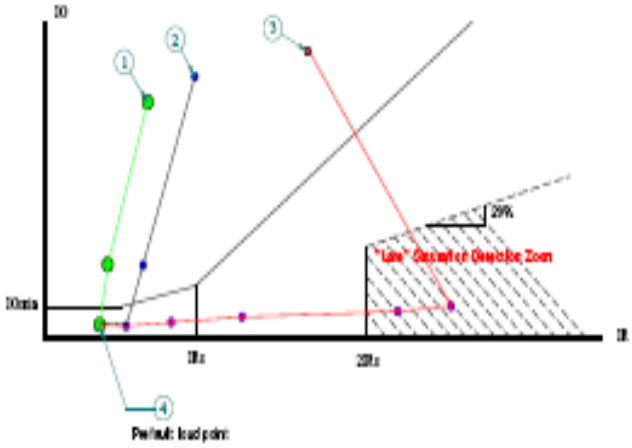


FIGURE 1: TRAJECTORY OF OPERATING (IO) AND RESTRAIN CURRENTS (IR)

The CT saturation detection algorithm is illustrated in Figure 1, in which 3 trajectories of IO vs. IR are displayed for (1) an internal fault, (2) an external fault with earlier CT saturation, i.e. saturation occurred in less than a cycle after the fault inception (could be in 1 or 2 ms after the fault inception). This case normally occurs with the extreme high fault current, and

(3) an external fault with late CT saturation, i.e. the saturation occurred in greater than one cycle (saturation could occur 2 or 3 cycles later after the fault inception). This case normally occurs with high DC component (the actual fault current may not be very high).

The early and late CT saturations are shown in Figure 2 and Figure 3 respectively.

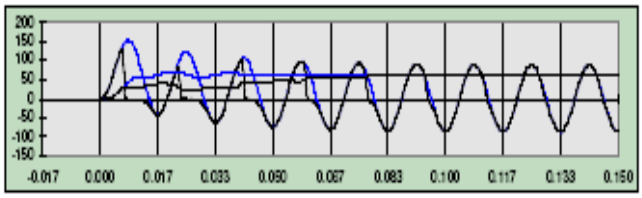


FIGURE 2: EARLY CT SATURATION

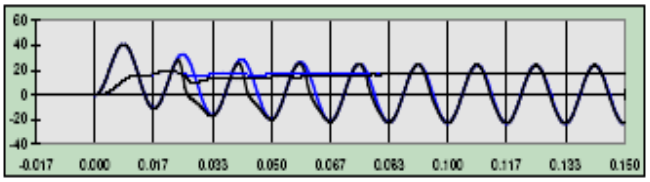


FIGURE 3: LATE CT SATURATION

The CT saturation detection algorithm contains two parts to deal with early CT saturation (curve 2 in figure 1) and late CT saturation (curve 3 in Figure 1) respectively.

2.1 Early CT saturation Detection

As shown in Figure 2, there is always a non-saturated part on the fault current waveform initially after the fault inception though this non-saturated part may only exist for a very short period of time. In the IO/IR plot, this initial non-saturated part represents the short movement of the trajectory along the IR axis in Figure 1 (curve (2)). An algorithm has been developed to detect this movement along IR axis (even though this movement may be very short) by comparing the angle difference between the second harmonics of the dIO/dt and the dIR/dt [5]. This algorithm has been proven to be extremely sensitive and effective to correctly detect any early/fast CT saturation by using the RTDS (Real Time Digital Simulator). Various test cases, including internal faults, external faults, arcing resistance, different load level, different CT burdens, etc., had been tested.

2.2. Late CT Saturation Detection

The above-described algorithm is only effective when the CT saturation occurs in the first cycle after the fault. It cannot detect the late CT saturation. The late CT saturation is detected by using the Block Zoon defined in Figure 1 (shadow area). This block zoon is bounded by IR=2*IRs and line with 20% of slope (see figure 1). Note that IRs (setting) should be set a little bit greater than the maximum bus transfer load (this guideline will be in the user's manual). For external fault with late CT saturation, the fault level must be high enough to make the IO/IR trajectory get into this zoon.

3.0 CT SATURATION DETECTION ALGORITHM

In the current investigation, the bus protection system includes a saturation detector that will detect all possible CT saturation conditions for external faults and block the differential protection from operating, when this condition prevails. The proposed method is immune to partial or fully offset waveforms, harmonics, fault arching resistance, capacitive or inductive loads, saturation (early or late), and saturation occurring during only a portion of a detected fault. This algorithm does not interfere with internal faults (with or without saturation) and performs the bus protection without sacrificing the speed and security.

An example of the fault current and the sum of non-fault currents at a bus needs to be protected is depicted in Figure 4.

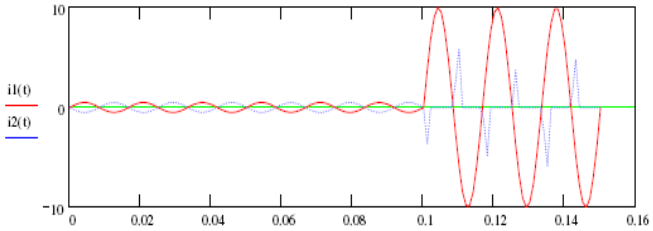


FIGURE 4: CURRENT SIGNALS (FAULT AND NO-FAULT): I1(t) – NO FALUT, I2(t)= FAULT PHASE WITH SATURATION

In a conventional way, from the sampled signal, fundamental phasors are estimated for operating (IO) or differential current and restrain current (IR) using the following relationship

$$IO(wn) := |I1(wn) + I2(wn)| \qquad IR(wn) := \frac{|I1(wn)| + |I2(wn)|}{2} \qquad \text{---(1)}$$

Where, wn= decimated sample count, and IO and IR are operating and retrain currents respectively. The following diagram shows the phasor traces.

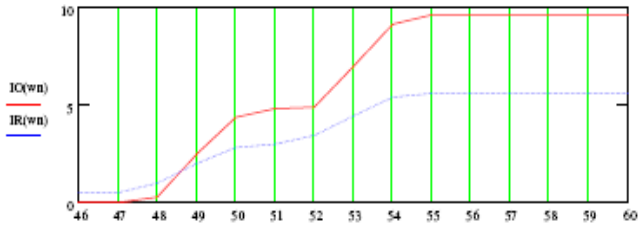


FIGURE 5: OPERATING (IO) and RESTRAIN (IR) CURRENTS ESTIMATED USING (1).

The rate of change of the operating current, and the restrain current is estimated to track the trajectory with respect to time as shown in Figure 6.

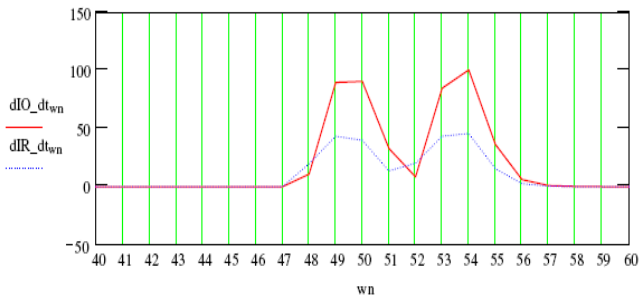
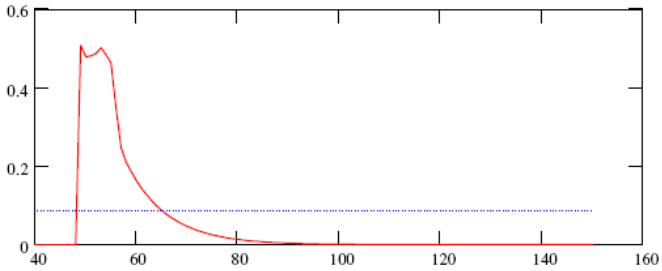


FIGURE 6: TRAJECTORY OF OPERATING CURRENT AND RESTRAIN CURRENT

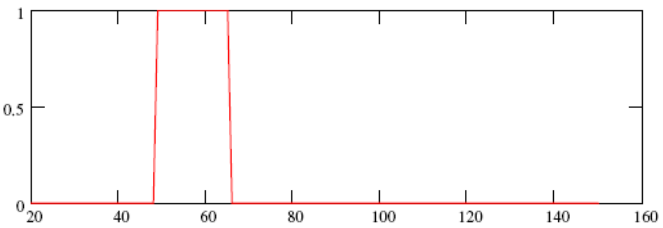
A second harmonic of the derivative expression as shown in Figure 6 is evaluated. In turn, the phase between the second harmonic of the derivatives of the operating current and restrain current is estimated and compared against the threshold value. For the above case, the resulting phase angle is depicted in Figure 7.



_____ Phase angle (radians)
---------- Threshold level
x-axis: Samples, y-axis: phase angle in radians

FIGURE 7: PHASE ANGLE ESTIMATATION AND COMPARISON AGAINST THRESHOLD

The performance of the saturation detector (block or non-block) is shown below.



x-axis: Samples , y-axis: binary decision (1- block)

FIGURE 8: ILLUSTRATION OF SATURATION DETECTOR PERFORMANCE

4.0 ADDITIONAL SECURITY FOR HIGH X/R SYSTEM

When the bus protection zone is connected with Generators and transformers, which exhibit high X/R ratio (30 ~ 100) , the system will experience a slow CT saturation, and the operating and restrain current trajectories exhibit different behavior. An additional security is provided for the conditions as referred in Figure 9.

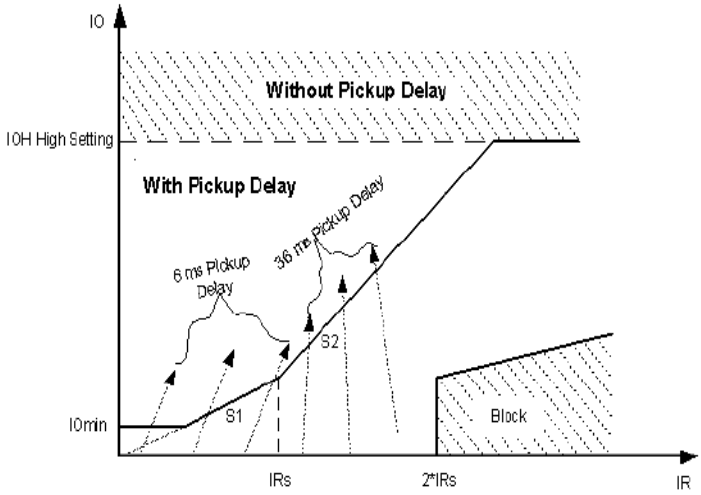


FIGURE 9: IO AND IR TRAJCETORY UNDER LATE CT SATURATION CONDITIONS

For additional security, some pickup delays are also applied to the differential protection function as described below.

4.1 IOmin and Slope1 (S1)

As shown in Figure 9, when the IO, IR trajectory enters into the trip zone from IOmin or slope1 region, a 6 ms (8 ms for 50Hz system) pickup delay is applied so as to be certain that the IO, IR trajectory has reliably come into the trip zone. To ensure the fast operating speed of 87B function for internal faults, IRs should be set to be greater than the maximum bus transfer load plus safety margin. The safety margin should be greater than S1/100 per unit. In this way, the IO, IR trajectories for internal faults are always entered into the trip zone from the IOmin and slope1 region rather than from the slope2 region under any pre-fault conditions.

4.2 Slope2 (S2)

When a slow CT saturation occurs during an external fault as described in section 2.2, the IO, IR trajectory may enter the trip zone, but always from the slope2 region. In most cases when the slow CT saturation occurs, the IO, IR trajectory will enter into the saturation block zone first so that the block flag will be set and 87B trip will be blocked accordingly. However, in some special situations when the fault current contains low

AC current combined with high magnitude slow decaying DC current, the external fault current level may not be high enough to bring the IO, IR trajectory into the saturation block zone, but it might still bring the IO, IR trajectory into the trip zone from slope2 region for a short period of time (the CT recovers to normal quickly). In order to make the relay secure under these special situations, a 36 ms (45ms for 50Hz system) pickup delay is applied. As described before, this delay does not affect the operating speed for internal faults.

4.3 IOH High Setting

There is no any intentional delay as long as the IO exceeds the IOH setting threshold no matter where the IO, IR trajectory comes from. The purpose of the IOH zone is to clear the extremely severe bus internal faults as soon as possible.

5.0 CONCLUSIONS

A novel CT saturation algorithm for bus differential protection has been presented and discussed. This algorithm has been well tested for all possible CT saturation and with additional security measures described; this algorithm is immune to partial or fully offset fault signals, harmonics, fault arching, and severity of CT saturation.

6.0 REFERENCES

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